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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,822	07/25/2001	Kiyoshi Nomura	SON-2164	6321

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,822	NOMURA ET AL.	
	Examiner	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,13 and 14* is/are rejected.

7)☐ Claim(s) *7-12 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 4, 10 and 15 objected to because of the following informalities:

It appears that claim 4 should be dependent on claim 2 instead of claim 1 because claim 4 includes the limitation "processing the received signal." There is no mention of a "received signal" in claim 1. However, claim 2 does introduce a "received signal."

In lines 6 and 11 of claim 10, the word "at" appears to be erroneously included.

In line 5 of claim 15, the word "at" appears to be erroneously included.

Appropriate correction is required.

Allowable Subject Matter

Claims 7-12 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al., US Patent no. 6,654,406 [Kim].

Kim discloses a clock supply circuit supplying a processing clock signal for processing an input signal having a predetermined frequency, said clock supply circuit comprising:

a clock generating means generating a first, higher frequency, clock signal and a second, lower frequency, clock signal [FIRST AND SECOND FREQUENCY GENERATORS in Figure 1]; and

a clock switching means for selecting any of the first or second clock signals and supplying the selected signal to the signal processing [SWITCH in Figure 1];
a clock switching control means processing said input signal with the use of the selected processing clock signal, detecting an amount out-of-sync of the processing clock signal in accordance with the processing result and controlling the clock switching in accordance with the detected out-of-sync [CONTROLLER in Figure 1 and column 3, lines 36-64].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., US Patent no. 6,529,548 [Aoki], in view of, Ogoro, US Patent no. 6,519,706.

Regarding claim 1, Aoki discloses a clock supply circuit comprising:

a first clock generating circuit for supplying a first clock signal [DCLK in Figure 4] having an almost fixed frequency to a first processing circuit [IrDA DEMOD. in Figure 4 and column 12, lines 5-9]; and

a second clock generating circuit for variably controlling the frequency of a second clock signal [CLK in Figure 4, column 7, lines 25-32 and column 12, lines 9-11] to a second processing circuit [CHARACTER DISCRIMINATOR in Figure 4].

Aoki does not disclose a load judgment means for judging a processing load of the second processing circuit and controlling the frequency of the second clock signal in accordance with a judgment result from the load judgment means. Ogoro discloses a load judgment means [arithmetic processing amount estimation unit] for judging a processing load of a digital signal processor [DSP] and controlling the frequency of the clock signal supplied to the DSP in accordance with a judgment result from the load judgment means [column 2, lines 56-60 and column 3, line 54 – column 4, line 10].

It would have been obvious to one of ordinary skill in the art to Adjusting the frequency of a clock signal supplied to the second processing circuit according to amount of processing load that is presented to the second processing circuit enables a reduction in the overall power consumption of the second processing circuit [Ogoro, column 1, lines 63-65].

Regarding claim 2, Aoki further discloses that the said first processing circuit includes a demodulation processing circuit [IrDA DEMOD. in Figure 4 and column 12, lines 5-9] for demodulating a received signal having a predetermined frequency transmitted through a channel, and generating a bit stream signal [column 12, lines 45-52], said second processing circuit includes a decoding processing circuit [CHARACTER DISCRIMINATOR in Figure 4] for

decoding said demodulated bit stream signal output from said demodulation processing circuit [column 7, lines 45-57].

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., US Patent no. 6,529,548 [Aoki] and Ogoro, US Patent no. 6,519,706, in view of, Nakatani, US Patent no. 6,188,258.

Aoki and Ogoro, as described above, disclose a clock supply circuit for supplying first and second clock signals to first and second processing circuits. Aoki and Ogoro do not explicitly disclose that the clock generation circuitry comprises a frequency multiplication circuit for multiplying a reference clock signal by a predetermined multiplication factor and first and second frequency dividers for dividing the multiplied clock signal to produce first and second clock signals that are supplied to the first and second processing circuits. However, Nakatani states that using a frequency multiplication circuit for multiplying a reference clock signal by a predetermined multiplication factor and using a plurality of frequency dividers for dividing the multiplied clock signal is a well-known method of generating a plurality of clock signals with frequencies that are different from an input reference clock signal [Figure 3 and column 2, lines 11-44]. It would have been obvious to one of ordinary skill in the art to use the well known method of using clock multiplication circuits and clock dividing circuits in the Aoki and Ogoro circuit in order to generate a plurality of clock signals with different frequencies from an input reference clock signal.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., US Patent no. 6,529,548 [Aoki] and Ogoro, US Patent no. 6,519,706, in view of, Kim et al., US Patent no. 6,654,406 [Kim].

Aoki and Ogoro, as described above, disclose a clock supply circuit for supplying first and second clock signals to first and second processing circuits. Aoki and Ogoro do not explicitly disclose detecting a timing deviation between the first clock signal and the received signal and compensating the timing of the first clock signal in accordance with the detected time deviation. Kim discloses a method comprising of selecting one of two different frequency clock signals to be supplied to a demodulation circuit. The selection is made based on the frequency of an input data signal [column 3, lines 36-64]. In summary, Kim discloses adjusting the frequency of a clock signal supplied to a demodulation circuit based on the frequency of an input data signal. It would have been obvious to one of ordinary skill in the art to use the Kim method in the Aoki and Ogoro system. Adjusting a demodulator operating frequency to match the frequency of the data signal input to the modulator enables the demodulator to process the input data signal more accurately.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., US Patent no. 6,654,406 [Kim], in view of, Bontekoe et al., US Patent no. 6,078,225 [Bontekoe].

Kim discloses a clock supply circuit supplying a processing clock signal for processing an input signal having a predetermined frequency, said clock supply circuit comprising:

a clock generating means generating a first, higher frequency, clock signal and a second, lower frequency, clock signal [FIRST AND SECOND FREQUENCY GENERATORS in Figure 1];

a clock switching means for selecting any of the first or second clock signals and supplying the selected signal to the signal processing [SWITCH in Figure 1]; and

a clock switching control means processing said input signal with the use of the selected processing clock signal, detecting an amount out-of-sync of the processing clock signal in accordance with the processing result and controlling the clock switching in accordance with the detected out-of-sync [CONTROLLER in Figure 1 and column 3, lines 36-64].

Kim discloses a clock supply circuit for generating and switching between two clock signals. Kim does not explicitly state that the circuit is capable of generating and switching between three clock signals instead of two clock signals. However, as shown by Bontekoe, switches for selecting between three clock signals are well known in the art [Figure 1 and column 2, lines 30-34]. It would have been obvious to one of ordinary skill in the art to modify the Kim clock supply circuit to support generating and switching between three clock signals instead of two clock signals to enable more accurate matching of the demodulator operating frequency and the input data signal.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., US Patent no. 6,654,406 [Kim], and Bontekoe et al., US Patent no. 6,078,225 [Bontekoe], in view of, Nakatani, US Patent no. 6,188,258.

Kim and Bontekoe, as described above, disclose a clock supply circuit for generating and selecting a clock signal to be supplied to a processing circuit. Kim and Bontekoe do not

explicitly disclose that the clock generation circuitry comprises a frequency multiplication circuit for multiplying a reference clock signal by a predetermined multiplication factor and a frequency division means for dividing the multiplied clock signal to produce a plurality of different frequency clock signals. However, Nakatani states that using a frequency multiplication circuit for multiplying a reference clock signal by a predetermined multiplication factor and using a plurality of frequency dividers for dividing the multiplied clock signal is a well-known method of generating a plurality of clock signals with frequencies that are different from an input reference clock signal [Figure 3 and column 2, lines 11-44]. It would have been obvious to one of ordinary skill in the art to use the well-known method of using clock multiplication circuit and clock dividing circuits in the Kim and Bontekoe circuit in order to generate a plurality of clock signals with different frequencies from an input reference clock signal.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., US Patent no. 6,654,406 [Kim], in view of, Nakatani, US Patent no. 6,188,258.

Kim, as described above, discloses a clock supply circuit for generating and selecting a clock signal to be supplied to a processing circuit. Kim does not explicitly disclose that the clock generation circuitry comprises a frequency multiplication circuit for multiplying a reference clock signal by a predetermined multiplication factor and a frequency division means for dividing the multiplied clock signal to produce a plurality of different frequency clock signals. However, Nakatani states that using a frequency multiplication circuit for multiplying a reference clock signal by a predetermined multiplication factor and using a plurality of frequency dividers for dividing the multiplied clock signal is a well-known method of generating a plurality of clock signals with frequencies that are different from an input reference clock signal [Figure 3

and column 2, lines 11-44]. It would have been obvious to one of ordinary skill in the art to use the well-known method of using clock multiplication circuit and clock dividing circuits in the Kim circuit in order to generate a plurality of clock signals with different frequencies from an input reference clock signal.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kakemizu et al., US Patent no. 6,728,926, discloses a selector for switching between more than two or more clock signals.

Osborn et al., US Patent no. 6,721,892, discloses adjusting the operating frequency of a circuit in accordance with the processing load of the circuit.

Williams, US Patent no. 5,774,704, discloses dynamically adjusting the operating frequency of a CPU according to the load placed on the CPU.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Paul Yanchus
February 9, 2005